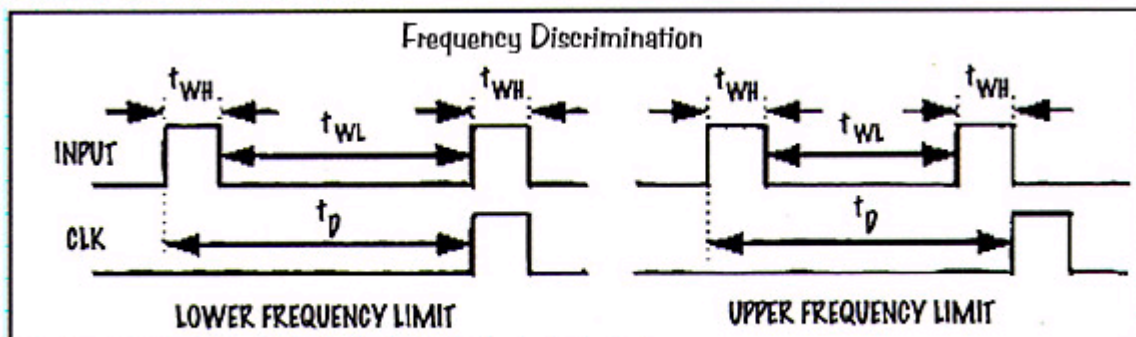**www.maxim-ic.com**

Spare Gates and Unused Delay Lines Can be Used to Build a Pulse Width Discriminator

The clock fail detector circuit can also be used with variable frequency clocks to determine if the clock frequency falls below, or rises above, a predetermined value.

Critical delay values are as follows:

In the case of a faster clock: $2t_{WH} + t_{WL}$

For a slower clock: $t_{WH} + t_{WL}$

For a 50% duty cycle clock: If $f_{IN} < 3 / (2t_D)$ or $f_{IN} > 1 / t_D$,   output = 1.

                                   If $1 / t_D > f_{IN} > 3 / (2t_D)$,   output = 0.

In fact, only the upper limit is duty cycle-dependent: the lower limit is always equal to the input period. The upper limit will be reduced for lower duty cycles (narrower input pulses) and increased for higher duty cycles (wider input pulses).

Note, however, that as the frequency is further increased or decreased, a point will occur when the output again returns to a zero state (when t_D corresponds to a low level on the input clock).
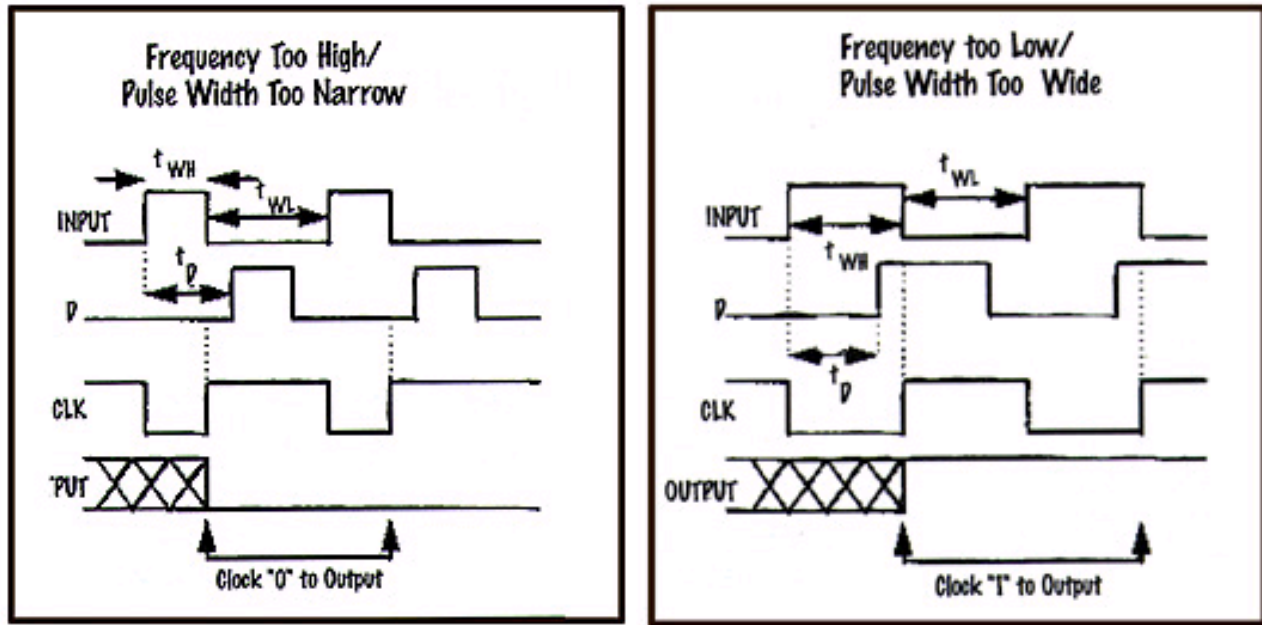
When it is required to detect a clock frequency that exceeds a certain value, this effect can be eliminated by a slight circuit modification: inverting the input signal to provide clock for the flip-flop and feeding the D input with the delayed input clock. (See *Detecting Clock Frequency Above Limit* diagram.) In this configuration, the maximum limit on clock frequency is reached when the input pulse width, t_{WH} or t_{WL}, becomes equal to the individual delay element value t_D.

In this configuration, the output state is dependent only on the width of the input clock (although both t_{WH} and t_{WL} must exceed the value of t_D), which allows the same circuit to be used for both frequency and pulse width detection.